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**1 Automatic generation of synthetic sequential benchmark circuits**

*Hutton, M.D.; Rose, J.S.; Cornell, D.G.;*

Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions ( , Volume: 21 , Issue: 8 , Aug. 2002

Pages:928 - 940

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**2 Characterization and parameterized generation of synthetic combinational benchmark circuits**

*Hutton, M.D.; Rose, J.; Grossman, J.P.; Cornell, D.G.;*

Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions ( , Volume: 17 , Issue: 10 , Oct. 1998

Pages:985 - 996

[\[Abstract\]](#)   [\[PDF Full-Text \(340 KB\)\]](#)   IEEE JNL

**3 Characterization and parameterized random generation of digital circuits**

*Hutton, M.; Grossman, J.P.; Rose, J.; Cornell, D.;*

Design Automation Conference Proceedings 1996, 33rd , 3-7 June 1996

Pages:94 - 99

[\[Abstract\]](#)   [\[PDF Full-Text \(620 KB\)\]](#)   IEEE CNF

**4 Generation of embedded RAMs with built-in test using object-oriented programming**

*Zimmermann, M.; Geilert, M.;*

Design Automation Conference, 1990. EDAC. Proceedings of the European , 12-March 1990

Pages:2 - 6

[\[Abstract\]](#)   [\[PDF Full-Text \(396 KB\)\]](#)   IEEE CNF

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☐ Check to search within this result set**Results Key:****JNL** = Journal or Magazine   **CNF** = Conference   **STD** = Standard**1 Behavioral synthesis of analog systems using two-layered design space exploration***Doboli, A.; Nunez-Aldana, A.; Dhanwada, N.; Ganesan, S.; Vemuri, R.;*  
Design Automation Conference, 1999. Proceedings. 36th, 21-25 June 1999  
Pages:951 - 957[\[Abstract\]](#)[\[PDF Full-Text \(788 KB\)\]](#)**IEEE CNF**[Home](#) | [Log-out](#) | [Journals](#) | [Conference Proceedings](#) | [Standards](#) | [Search by Author](#) | [Basic Search](#) | [Advanced Search](#) | [Join IEEE](#) | [Web Account](#) | [New this week](#) | [OPAC Linking Information](#) | [Your Feedback](#) | [Technical Support](#) | [Email Alerting](#) | [No Robots Please](#) | [Release Notes](#) | [IEEE Online Publications](#) | [Help](#) | [FAQ](#) | [Terms](#) | [Back to Top](#)

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☒ 1. Document ID: US 20030208723 A1

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File: PGPB

Nov 6, 2003

PGPUB-DOCUMENT-NUMBER: 20030208723

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20030208723 A1

TITLE: Automated processor generation system for designing a configurable processor and method for the same

PUBLICATION-DATE: November 6, 2003

INVENTOR-INFORMATION:

| NAME                    | CITY            | STATE | COUNTRY | RULE-47 |
|-------------------------|-----------------|-------|---------|---------|
| Killian, Earl A.        | Los Altos Hills | CA    | US      |         |
| Gonzalez, Ricardo E.    | Menlo Park      | CA    | US      |         |
| Dixit, Ashish B.        | Mountain View   | CA    | US      |         |
| Lam, Monica             | Menlo Park      | CA    | US      |         |
| Lichtenstein, Walter D. | Belmont         | MA    | US      |         |
| Rowen, Christopher      | Santa Cruz      | CA    | US      |         |
| Ruttenberg, John C.     | Newton          | MA    | US      |         |
| Wilson, Robert P.       | Palo Alto       | CA    | US      |         |
| Wang, Albert Ren-Rui    | Fremont         | CA    | US      |         |
| Maydan, Dror Eliezer    | Palo Alto       | CA    | US      |         |

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☒ 2. Document ID: US 6671818 B1

L14: Entry 2 of 4

File: USPT

Dec 30, 2003

US-PAT-NO: 6671818

DOCUMENT-IDENTIFIER: US 6671818 B1

TITLE: Problem isolation through translating and filtering events into a standard object format in a network based supply chain

| Full | Title | Citation | Front | Review | Classification | Date | Reference | References | Abstracts | Claims | KIMC | Draw. De |
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☒ 3. Document ID: US 6606744 B1

L14: Entry 3 of 4

File: USPT

Aug 12, 2003

US-PAT-NO: 6606744

DOCUMENT-IDENTIFIER: US 6606744 B1

TITLE: Providing collaborative installation management in a network-based supply chain environment

| Full | Title | Citation | Front | Review | Classification | Date | Reference | References | Abstracts | Claims | KIMC | Draw. De |
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☐ 4. Document ID: US 6477683 B1

L14: Entry 4 of 4

File: USPT

Nov 5, 2002

US-PAT-NO: 6477683

DOCUMENT-IDENTIFIER: US 6477683 B1

TITLE: Automated processor generation system for designing a configurable processor and method for the same

| Full | Title | Citation | Front | Review | Classification | Date | Reference | References | Abstracts | Claims | KIMC | Draw. De |
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